ABSTRACT OF THE DISCLOSURE

A power semiconductor device having a low on-resistance and a high breakdown ruggedness is disclosed. Trench regions formed so as to contact trench gates via gate-insulating films are connected by emitter regions so as to form a ladder-shaped configuration. The emitter regions are formed at a shallower depth than the trench regions. Therefore, the resistance in portions of the body that are near the interfaces with the emitter regions is reduced, and the operation of parasitic transistors formed by the emitter regions, the body, and an epitaxial layer is substantially prevented. As a result, the on-resistance is varied, and the avalanche ruggedness and the latch-up ruggedness are improved.

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